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A Novel Electro-Thermal Model for Wide Bandgap Semiconductor Based Devices

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Keywords

«Electro-Thermal Model», «Thermal coupling», «Junction-Case temperature estimation», «Thermal Cycling», «Safe Operation Area».

Abstract

This paper propose a novel Electro-Thermal Model for the new generation of power electronics WBG-devices (by considering the SiC MOSFET-CMF20120D from CREE), which is able to estimate the device junction and case temperature. The Device-Model estimates the voltage drop and the switching energies by considering the device current, the off-state blocking voltage and junction temperature variation. Moreover, the proposed Thermal-Model is able to consider the thermal coupling within the MOSFET and its freewheeling diode, integrated into the same package, and the influence of the ambient temperature variation. The importance of temperature loop feedback in the estimation accuracy of device junction and case temperature is studied. Furthermore, the Safe Operating Area (SOA) of the SiC MOSFET is determined for 2L-VSI applications which are using sinusoidal PWM. Thus, by considering the heatsink thermal impedance, the switching frequency and the ambient temperature, the maximum allowed drain current is determined according to the thermal limitations of the device. Finally, dynamic study of MOSFET junction and case temperature is also performed by considering the variation of the ambient temperature and of the load current.

Introduction

The converter availability in the application is the most important aspect which depends on the component reliability, efficiency and its maintenance. Therefore, highly reliable components are required in order to minimize the downtime during the lifetime of the converter and implicitly the maintenance costs [1],[2]. Temperature is the most important stressor which involves failure among the converter components, especially in semiconductor devices, capacitors and PCBs [3],[4]. Therefore, the maximum electrical ratings and the thermal limitations of the semiconductor devices plays a key role in the robustness design and reliability of power electronics converters [1].
The producers should guarantee that under all mentioned operating conditions, the case and junction temperature of all devices do not exceed their designed physical limits otherwise, it may involve failures of the product [5]. This problem has a higher impact for the new generation of power converters based on WBG-devices, due to their superior Electro-Thermal properties which involves a higher temperature operating point, compared to the Si-based devices [6]. Therefore, it is important to carry out a thermal loading analysis of the devices, in order to determine if they are performing within the maximum allowed physical limits, especially for the worst case scenario. This paper deals with a novel Electro-Thermal Model which estimates the device parameters by considering also the temperature impact, the ambient temperature variation, the thermal-coupling between MOSFET-Diode and the heatsink thermal impedance for PWM controlled 2L-VSI.

Proposed Electro-Thermal Model

The Electro-Thermal Model deals with the analysis of both electrical and thermal performances, which interacts with each other by the power dissipation of the electronics devices [7].

The main goal of the proposed model is to estimate the junction and case temperature for the new generation of power electronics devices. The Electro-Thermal Model has been implemented for the SiC diode (C4D20120A) and MOSFET (CMF20120D) from CREE in Matlab/Simulink by using M-functions. According with Fig. 1, three types of models are involved in the electro-thermal analysis: the device model, the power loss model and the thermal model.

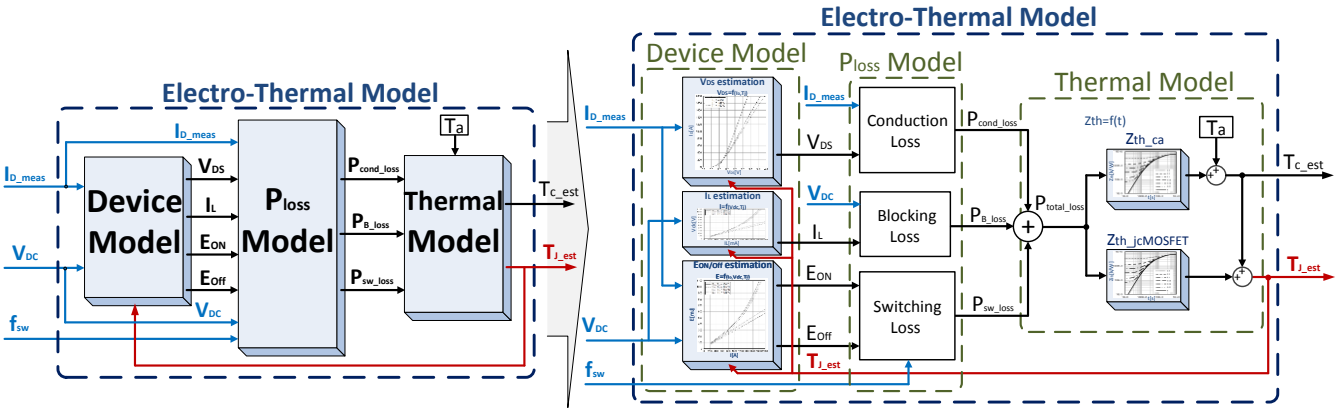


Fig. 1: Proposed Electro-Thermal model structure for device junction and case temperature estimation

Device model

The main purpose of the Device-Model is to estimate the voltage drop across the device, the leakage current and the switching energies as a function of the current, the off-state blocking voltage and junction temperature. Furthermore, the estimated parameters and the switching frequency will be used into the P_{Loss} Model where, the instantaneous conduction (P_C), blocking/leakage (P_B) and switching losses (P_{SW}) of the device are calculated. Moreover, the total losses (P_{tot_loss}) and the ambient temperature are feed into the thermal model which estimates the device case and the junction temperature. Finally, by providing the junction temperature as a feedback to the device model, the temperature impact is considered. The total losses (P_{tot_loss}) of the device are given by:

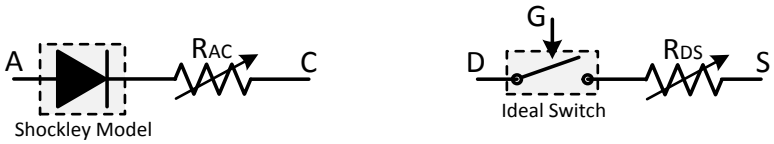
$$P_{tot\_loss} = P_C + P_{SW} + P_B \tag{1}$$

Conduction losses

The MOSFET (diode) conduction losses are produced by the on-state drain-source (forward) voltage drop V_{DS} (V_F) across the power device and the instantaneous value of the current I_D (I_F), which is flowing through it. As shown in Fig. 3, they occur only during the on-state of the device and they are calculated as:

$$P_C(t) = \frac{1}{T_{on}} \int_{Toff}^{Toff+Ton} v_{DS}(t) \cdot i_D(t) dt \tag{2}$$

The current I_D (I_F) is known thus, the V_{DS} (V_F) has to be estimated in order to have an accurate calculation of the conduction losses. The on-state voltage is related to the device current and the junction temperature variations.



(a)Diode Model (b)MOSFET model

Fig. 2: Proposed Shockley-based diode model (a) and MOSFET model (b) by considering also the internal resistance variation

In order to achieve an accurate estimation of the diode forward voltage drop V_F in the whole working area, the Shockley model [8] in combination with the resistance model is proposed (Fig. 2(a)). Therefore, the used equation for diode on-state voltage drop estimation has the following form:

$$V_F = n \cdot V_{Th} \cdot \ln\left(\frac{I_F}{I_S} + 1\right) + R_{AC} \cdot I_F \tag{3}$$

Where n=4 is a constant which has been determined in order to improve the estimation accuracy of the on-state voltage V_F. Furthermore, the thermal voltage V_{Th}, the saturation current I_S and the on state resistance R_{AC} are modeled as a function of the junction temperature T_j. The V_{Th} estimation according with T_j variation, is achieved by implementing (4) where $k=1.38\cdot10^{-23}$J/K is the Boltzmann constant and $q=1.60\cdot10^{-19}$J/V is the elementary electron charge.

$$V_{Th} = \frac{k \cdot T_j}{q} \tag{4}$$

Moreover, the saturation current I_S is determined by considering:

$$I_S = \alpha \cdot e^{\frac{T_J - T_{ref}}{\beta}} \tag{5}$$

Where α and β are found by applying the least square method considering the values available from the datasheet graph for different temp curves.
Finally the on-state resistivity variation according with the temperature is obtained in (6).

$$R = \left[a \cdot \left(T_j - T_{ref}\right) + 1\right] \cdot R_0 \tag{6}$$

Where R_0 is the initial resistance at temperature T_{ref}, a is the temperature coefficient and T_{ref} is the reference temperature for which a is mentioned.
The MOSFET is modeled as an ideal switch in series with a resistance (Fig. 2 (b)). Thus, in order to include the on state drain source resistance variation as a function of T_j, the equation (6) is used. Therefore, the MOSFET on-state voltage drop estimation is performed as:

$$V_{DS} = I_D \cdot \left[a \cdot \left(T_j - T_{ref}\right) + 1\right] \cdot R_0 \tag{7}$$

Finally, the obtained parameters values for the mentioned devices are emphasized in Table I.

Table I: Diode and MOSFET models parameters

SiC Devices from CREE	Parameters		
	On-state resistance	Saturation current	Thermal voltage
Diode C4D20120A	$R_{AC} = \left[0.01177 \cdot \left(T_j - 273.15\right) + 1\right] \cdot 0.019$	$I_S = 0.00042 \cdot e^{\frac{T_J - 273.15}{25.2}}$	$V_{Th} = \frac{1.38 \cdot 10^{-23} \cdot T_j}{1.6 \cdot 10^{-19}}$
MOSFET CMF20120D	$R_{DS} = \left[0.00407 \cdot \left(T_j - 273.15\right) + 1\right] \cdot 0.07356$	-	-

Blocking losses

The MOSFET blocking losses are produced by the leakage current I_{LM} and the off-state blocking voltage V_{DD} of the power device. They occur only during the off-state time of the device and they are calculated using:

$$P_B(t) = \frac{1}{T_{off}} \int_{Ton}^{Ton+Toff} v_{DD}(t) \cdot i_L(t) dt \tag{8}$$

The leakage current depends on the blocking voltage capability and the temperature of the semiconductor chip. The value of this current is very low, therefore, these losses can be neglected, but for improving the model accuracy, they are considered in this paper. The same procedure is applied when calculating the conduction and P_B of the diode. The main difference is that for conduction losses are considered the on-state forward voltage V_F of the diode and its freewheeling current I_F, and for blocking losses are considered the leakage current of the diode I_{LD} and its reverse blocking voltage V_R.

Switching losses

When a transition from OFF to ON (or opposite) is performed, the voltage and the current do not change instantaneously. There is a transient period, emphasized in Fig. 3, which produces the P_{sw}. These losses are related to the off-state blocking voltage V_{DD}, the instantaneous drain current I_D, the switching frequency f_{SW} and the T_j. They are calculated using the equation (9).

$$P_{SW} = (E_{on} + E_{off}) \cdot f_{SW} \tag{9}$$

In equation (9) E_{on} and E_{off} represent the turn-on and turn-off energies. These energies are not easy to calculate, since they depend on the dynamics of the commutation process. The estimation of the E_{on} and E_{off} is done by using the equations (10) and (11).

$$E_{on} = \int_0^{t_{ri}+t_{fv}} v_{DS}(t) \cdot i_D(t) dt = E_{onM} + E_{onDrr} = V_{DD} \cdot I_D \frac{t_{ri} + t_{fv}}{2} + Q_{rr} \cdot V_{DD} \tag{10}$$

$$E_{off} = \int_0^{t_{rv}+t_{fi}} v_{DS}(t) \cdot i_D(t) dt = V_{DD} \cdot I_D \frac{t_{rv} + t_{fi}}{2} \tag{11}$$

where t_{ri}-rising time of the current, t_{fv}-falling time of the voltage, t_{rv}-rising time of the voltage, t_{fi}-falling time of the current and Q_{rr}-reverse recovery charge of the diode.

The current I_D which is flowing through the device and the V_{DD} are known thus, in order to have an accurate calculation of E_{on} and E_{off}, the parameters that have to be estimated are the commutation times t_{ri}, t_{fv}, t_{rv}, t_{fi} and the Q_{rr} of the diode. Actually, the turn-on and turn-off switching times (12) are changing according with the off-state blocking voltage, drain current and junction temperature variations. The calculation of the commutation times is done according with Table II.

$$t_{r/f(i,v)} = f(V_{DD}, I_D, T_J),\ V_{DD} = 0\ \ to\ \ 1200V,\ \ I_D \in 0\ \ to\ \ 40A,\ \ T_J = 25\ \ and\ \ 125°C \tag{12}$$

Table II: Turn-on and turn-off commutation time

	Current	Voltage
Rise time (t_r)	$t_{ri} = R_G \cdot C_{ISS} \cdot \ln\left(\frac{V_{GSon} - V_{th}}{V_{GSon} - V_{pl}}\right)$	$t_{rv} = \frac{Q_{GD}}{I_{Goff}}$ where $I_{Goff} = \frac{-V_{pl}}{R_G}$
Fall time (t_f)	$t_{fi} = R_G \cdot C_{ISS} \cdot \ln\left(\frac{V_{pl}}{V_{th}}\right)$	$t_{fv} = \frac{Q_{GD}}{I_{Gon}}$ where $I_{Gon} = \frac{V_{GSon} - V_{pl}}{R_G}$

Moreover the gate-drain charge Q_{GD} is calculated by considering equation (13).

$$Q_{GD} = C_{GD}(V_{DD} - V_{DS}) \ \text{ for } \ C_{GD} = \frac{C_{GD1} + C_{GD2}}{2} \tag{13}$$

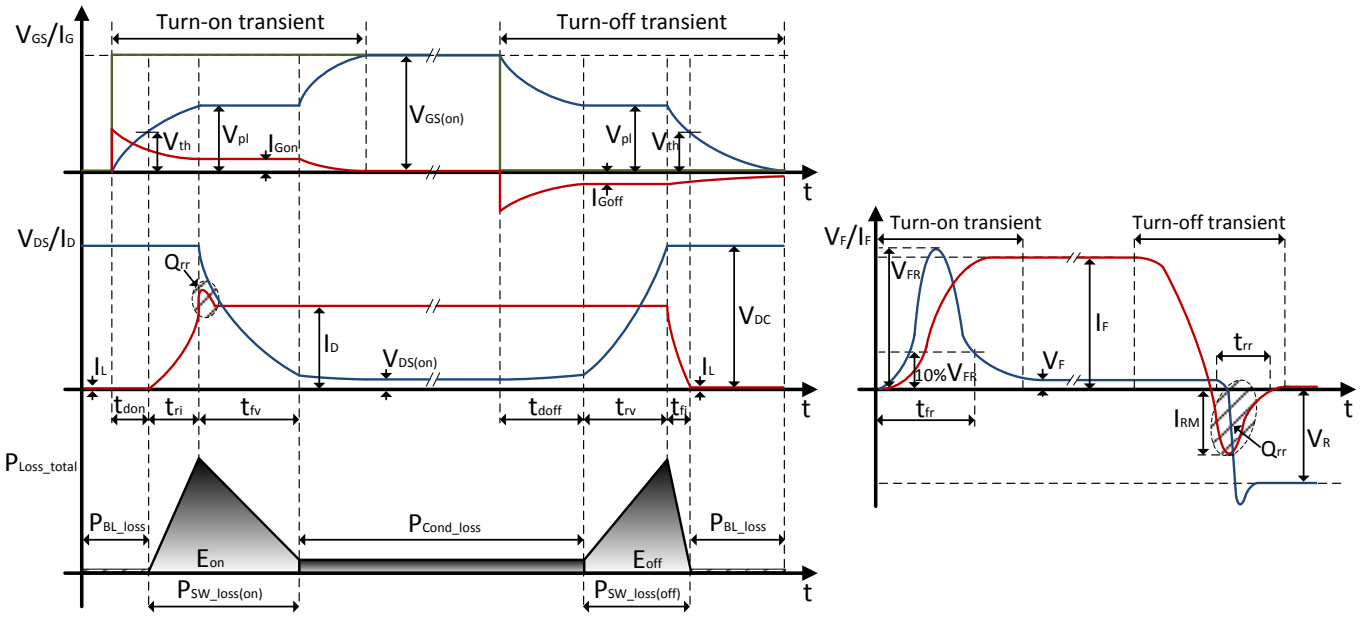
In the device datasheet is provided the typical dependence of the gate-drain capacitance C_{GD} on the drain-source voltage V_{DS}. In order to calculate the voltage rise and fall times with a reasonable accuracy, the non-linearity of C_{GD} has to be taken into account, thus, a two point approximation is used:

- If $V_{DS} \in [0, V_{DD}/2]$, then the gate-drain capacitance takes value according with the on-state voltage drop variation, $C_{GD1}=C_{GD}(V_{DS})$.
- For $V_{DS} \in [V_{DD}/2, V_{DD}]$, the gate-drain capacitance takes value of $C_{GD2}=C_{GD}(V_{DD})$.

In Table II, it can be noticed that the threshold V_{th} and Miller plateau voltage V_{pl} are of major importance, influencing the switching characteristic in terms of rise and fall times of the MOSFET voltage and current. Therefore, special attention is given to the estimation of V_{pl} and V_{th} considering the drain current variation and the temperature impact. The proposed method relies on the typical transfer characteristics curves mentioned in datasheet. Afterwards, two points belonging to the same temperature curve are chosen and their corresponding drain current (I_{D1} and I_{D2}) and gate-source voltage (V_{GS1} and V_{GS2}) are used. Furthermore, the V_{th} and V_{pl} are calculated according with the equations (14). The same procedure is applied when the calculation is performed for the second temperature curve. Finally, by using the proposed method, the switching losses can be estimated for different current levels, considering also the temperature influence.

$$V_{th} = \frac{V_{GS1} \cdot \sqrt{I_{D2}} - V_{GS2} \cdot \sqrt{I_{D1}}}{\sqrt{I_{D2}} - \sqrt{I_{D1}}} \quad \text{and} \quad V_{pl} = V_{th} + \sqrt{\frac{I_D}{K}}$$
$$\text{Where} \quad I_{D1} = K \cdot (V_{GS1} - V_{th})^2 \Rightarrow K = \frac{I_{D1}}{(V_{GS1} - V_{th})^2} \tag{14}$$

When dealing with diode switching losses estimation, a different approach has to be considered. The minority carriers, which have flooded the PN-junction during the on-state phase, must be removed before the diode can start to block the reverse voltage. This reverse recovery current, not only determines the turn-off losses of the diode, but also will be absorbed by the MOSFET, causing its additional turn-on losses.



(a) MOSFET switching transients (b) Diode switching transient

Fig. 3: Turn-on and turn-off switching waveforms and energy losses of the device

The current rise time of the diode is determined by the turn-off time of the MOSFET and the load current, which determines the dI_F/dt.

The datasheet of the studied device shows also the turn-on recovery time t_{fr} and the turn-on overvoltage V_{FR} according with dI_F/dt variation. Thus, the t_{fr} and V_{FR} are determined according with dI_F/dt variation. Finally, the turn-on energy E_{on} is calculated as:

$$E_{on} = I_F \cdot V_{FR} \cdot t_{fr} \tag{15}$$

The current fall time of the diode is determined by the turn-on time of the MOSFET and the load current, resulting that dI_F/dt calculation considers the temperature impact. Moreover, the reverse-recovery peak current I_{RM} and the reverse-recovery time t_{rr} are chosen from the datasheet according with the dI_F/dt variation.

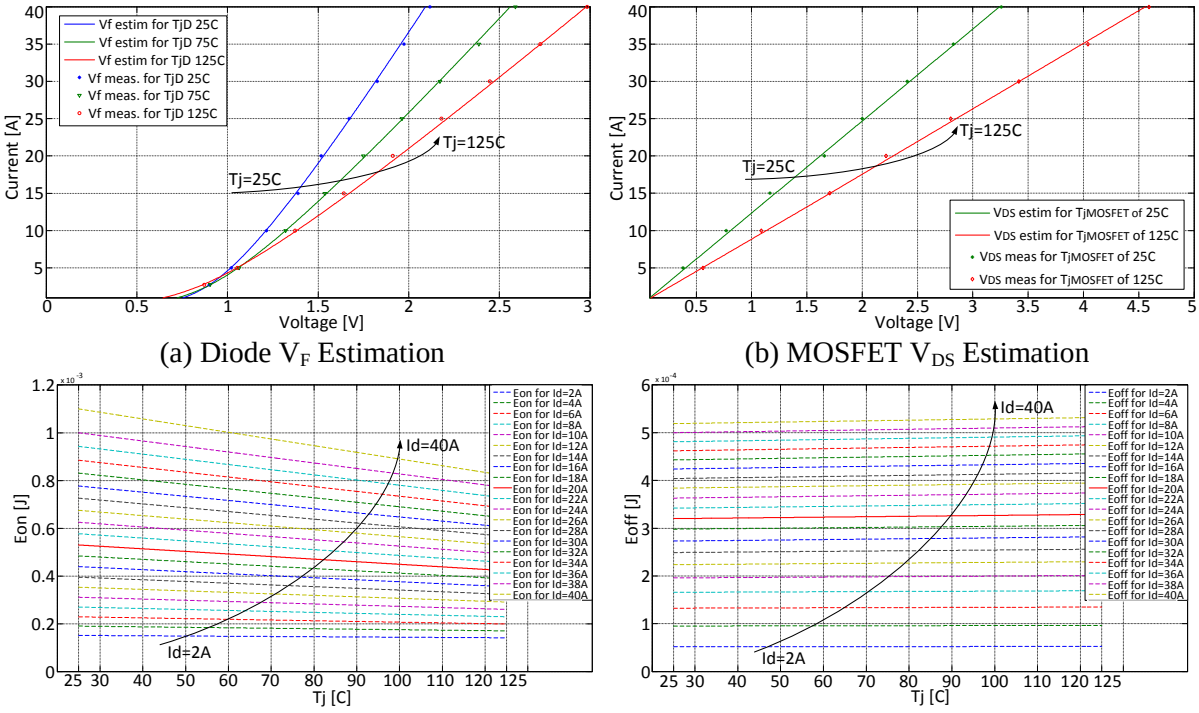
$$E_{off} = I_{RM} \cdot V_R \cdot t_{rr} \tag{16}$$

It is worth to mention that the device datasheet provides typical output characteristics graphs which emphasize the t_{fr}, V_{FR}, t_{rr} and I_{RM} according with dI_F/dt for two junction temperatures, 25°C and 125°C respectively. Therefore, the diode commutation energies were calculated for two different temperature curves. By performing the interpolation within the mentioned curves, it is possible to estimate the energies for different junction temperature levels than the mentioned ones. Finally, the turn-on and turn-off power losses are calculated by multiplying the pulse energies with the switching frequency.

Device model validation

The proposed Electro-Thermal Model has been implemented for the mentioned devices in Matlab/Simulink by using M-functions. The device model validation has been made by comparing the obtained simulation results with the experimental values from the device datasheet, by applying the same conditions.

Fig. 4 (a) and (b) presents the V_F (a) and V_{DS} (b) estimation when the current is increased from 0A to 40A, for junction temperature values between 25°C and 125°C. According to the obtained results, it is worth to mention that the model is performing a good estimation in the whole working area, the largest deviation from the read points in the datasheet being of 2 %. Furthermore, Fig. 4 (c) and (d) presents the MOSFET estimated switching energies E_{on} (c) and E_{off} (d) when the junction temperature is increasing from 25°C to 125°C for current levels between 2A and 40A with steps of 2A and for a constant V_{DD} of 800V. Also for this case were obtained similar values of energies with those provided by the datasheet when the same conditions were considered.



(a) Diode V_F Estimation (b) MOSFET V_{DS} Estimation

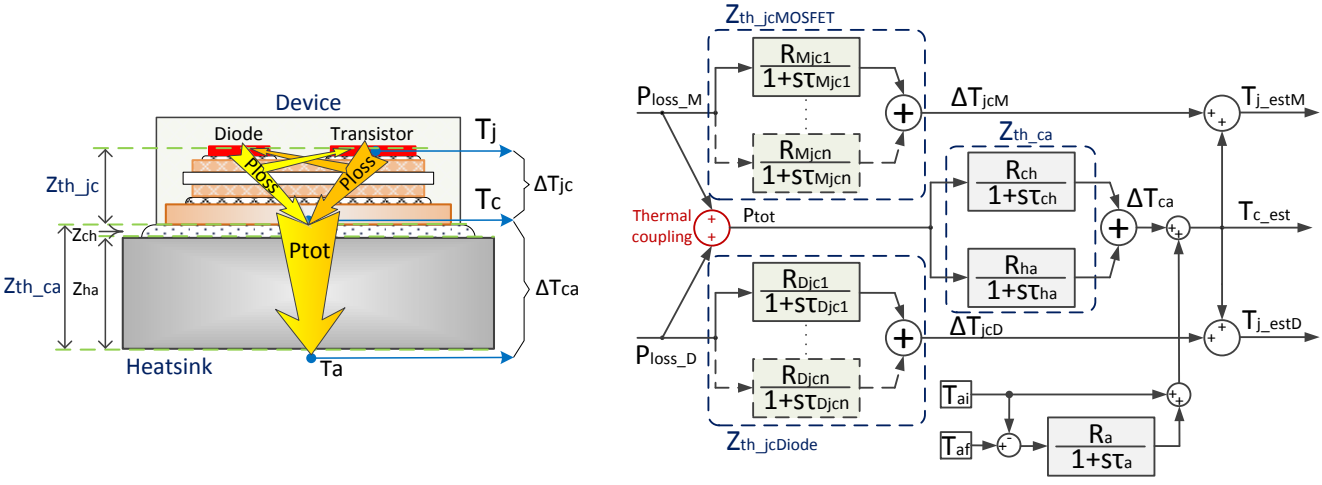
(c) MOSFET E_{on} Estimation (d) MOSFET E_{off} Estimation

Fig. 4: Estimation of diode (a) and MOSFET on-state voltage drop (b) and of MOSFET switching energies E_{on} (c) and E_{off} (d) when the current is increased from 0A to 40A and the junction temperature is increasing from 25°C to 125°C

Thermal model

The studied case presents the discrete device CMF20120D from CREE which has the transistor MOSFET and the freewheeling diode integrated on the same package (TO-247). Physically, (Fig.5(a)) the transistor and diode power losses flow through separate ways from their own junction to the baseplate, where temperatures are equal for contacting the same case. Afterwards, they merge together and flow through the heatsink and dissipate to the ambient.

In order to achieve a good estimation of the junction and case temperatures, there are three main aspects that should be considered in the thermal model. The device case temperature is a consequence of the total loss (P_{tot}) produced by the transistor and diode. The temperature of the transistor chip (respectively diode) varies also due to the diode chip losses (transistor chip losses). The impact of the ambient temperature variations need to be considered.



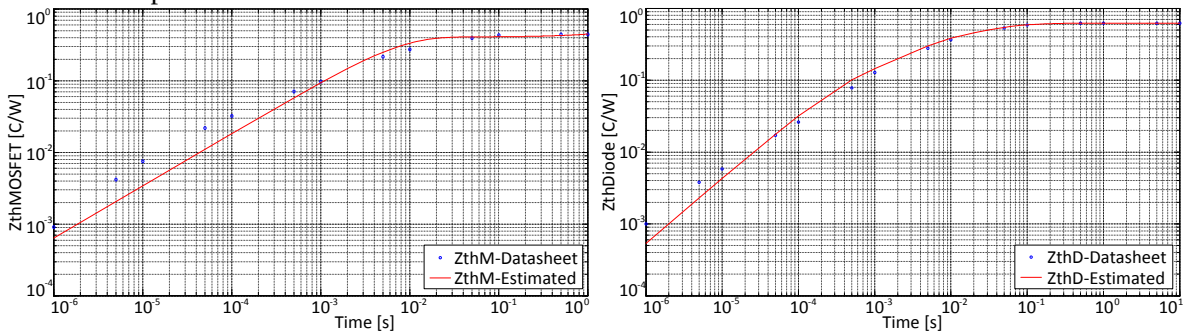
(a) Physically internal structure of the device (b) Proposed Thermal Model Structure

Fig. 5: Heat dissipation through the internal structure of the device (a) and proposed thermal model structure (b)

Those aspects are included in the proposed model due to the thermal coupling of the MOSFET and diode losses. Thus, according to Fig. 5 (b), T_c is determined by the device P_{tot}, and the MOSFET (Diode) T_j is influenced also by diode (MOSFET) power losses. The thermal impedance and temperatures across the device are emphasized in Fig. 5 (a). R_{jc} is the junction-case thermal resistance while R_{ch} and R_{ha} are the thermal resistance of the thermal grease and heatsink respectively.

$$Z_{th\_jc} = \sum_{i=1}^{n} R_i \cdot (1 - e^{\frac{-t}{\tau_i}}) \tag{17}$$

To estimate the thermal impedance of the device, first order transfer functions are used. The R_{jc} and τ_{jc} parameters are determined by implementing (17) in the CFTOOL from Matlab in order to estimate the thermal impedance curve provided in the device datasheet according to Fig. 6. It is worth to mention that a number of four parameters are more than sufficient for a good estimation of the Cauer Network. The obtained parameters for the device can be seen in Table III.



(a)Thermal impedance of the MOSFET (b) Thermal impedance of the Diode

Fig. 6: Thermal impedance estimation of the device by considering the transistor and its freewheeling diode

Table III: Device Thermal Impedance Parameters Estimation

	MOSFET+D-CREE(SiC)			
	MOSFET		Diode	
No.	R_{thM}[K/W]	τ_{Mjc}[s]	R_{thD}[K/W]	τ_{Djc}[s]
1.	0.1225	7.7e-4	9.634e-5	3.692
2.	0.3003	1.547e-2	0.01513	3.67
3.	0.5574	37.43	0.2524	1.536e-3
4.	0.565	31.05	0.3576	3.271e-2

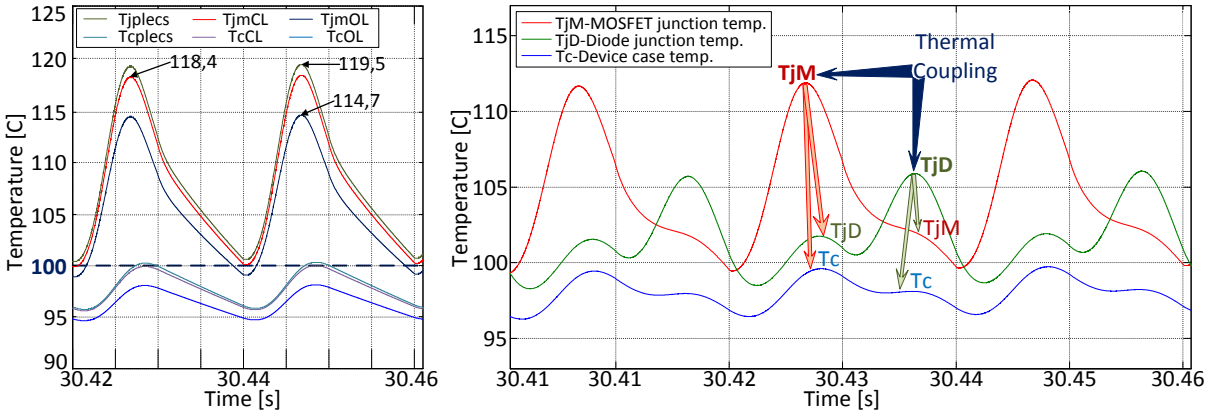
Moreover, by applying device P_{tot} as input to the MOSFET/diode estimated Z_{th} the ΔT_{jc} is obtained. Applying P_{tot} to the Z_{th_ca} the temperature ΔT_{ca} is achieved. The ambient temperature variation from its initial value T_{ai}=25°C to the final value T_{af}=30°C is also considered. Finally, the T_c and T_j of the device are determined by using the following equations (18).

$$\begin{aligned} T_c &= \Delta T_{ca} + T_a \\ T_j &= \Delta T_{jc} + T_c \end{aligned} \tag{18}$$

Another important aspect in the thermal model design is the heatsink thermal impedance (Zth_ha). The Zth_ha has been calculated for the following conditions: I_D=22A, f_{sw}=50kHz, the maximum ambient temperature T_{af}=30°C and the device case temperature should not exceed its maximum allowed physical limits of T_c=100°C. The obtained value for the heatsink thermal impedance is R_{ha}=3[K/W] and the time response is τ_{ha}=12s. Additionally, the values for the thermal grease were considered according with the data provided by the manufacturer which includes the material properties, the layer width and the commune contact surface of the device-heatsink connection as R_{ch}=0.0026 [K/W] and a time response of τ_{ch}=0.01s.

Simulation results

Considering all the above mentioned specifications, the proposed Electro-Thermal Model of the SiC-MOSFET from CREE (CMF20120D), has been implemented in Matlab/Simulink by using M-functions. The proposed model is validated by comparing it with a model built in Matlab/Simulink and Plecs toolbox, when the same conditions are applied. A structure of a sinusoidal pulse width modulation (PWM) for two level voltage source inverter with a switching frequency of 50kHz is used. The peak current is I_D=22 A, the voltage applied across the device is V_{DD}=800 V, the heatsink thermal impedance of Z_{th}=3 [K/W] and finally the ambient temperature of Ta=30°C. Fig. 7 (a) presents a comparison study between the MOSFET thermal cycling estimation obtained with the proposed model (considering also the closed loop temperature feedback) T_{jmCL} (red signal) and with the Plecs model T_{jplecs} (green signal). According with the Fig. 7 (a) can be stated that the obtained results with both models are very similar, the estimated peak temperature is with 1.1°C higher in case of the Plecs model. Moreover, in order also to study the influence of the parameters variation once with the temperature variations, a case study which is not considering the temperature loop feedback has been performed (and the results are emphasised with blue line signal). When analysing the obtained results, Fig. 7 (a) shows that the estimated junction peak temperature in open loop (blue signal) is with 3.7°C lower than in closed loop (red signal). This difference will have an impact from the reliability studies point of view. Therefore, to improve the accuracy of the model it is very important to consider also the temperature loop feedback. In order to emphasise the thermal coupling between MOSFET and its freewheeling diode, a case study have been performed by considering that the current stress which is flowing through the MOSFET is equal with the reverse current which flows through the diode. Fig. 7 (b) shows that the Diode/MOSFET junction chip temperature varies also due to MOSFET/Diode losses, and the device case temperature Tc varies due to P_{tot}, therefore MOSFET-Diode thermal coupling was achieved by implementing the proposed model.



(a) Model Validation (b) Thermal coupling within MOSFET and freewheeling diode

Fig. 7: Thermal loading comparison within the proposed model and a model built in Plecs toolbox (a) and the thermal coupling influence within MOSFET and its freewheeling diode (b)

Fig.8 presents the safe operating area (SOA) of the SiC MOSFET-CMF20120D from CREE by considering the maximum allowed drain current according with the switching frequency and heatsink thermal impedance variation. The calculated SOA is performed for 2L-VSI applications which are using sinusoidal PWM. In order to determine the SOA limits, the following parameters are provided as input to the model: drain current I_D, the voltage is constant V_{DD}=800 V, the power factor is cos φ=1, the switching frequency f_{sw} varies from 10 kHz to 100kHz according with the study case, the heatsink thermal impedance Z_{th} which can be 2 K/W, 3 K/W or 5 K/W, the ambient temperature which is considered constant at T_a=30°C, and the thermal limitations of the device in terms of case and junction temperature T_c=100°C and T_j=135°C. By considering the heatsink thermal impedance (2 K/W, 3 K/W or 5K/W) and a certain switching frequency(from 10 kHz to 100 kHz) according with the study case, the maximum allowed drain current is determined in order to not exceed the thermal limitations of the device.

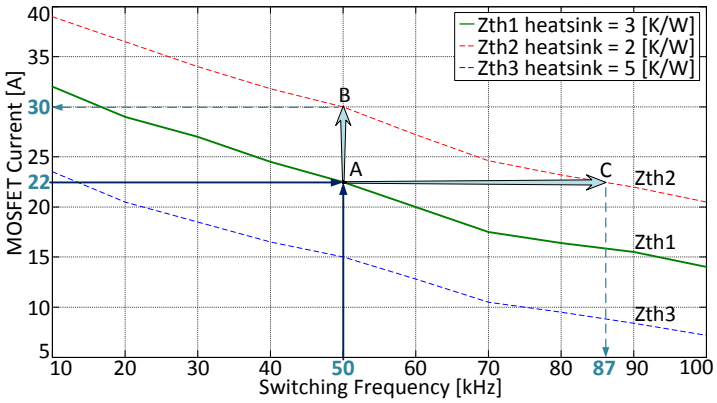


Fig. 8: Safe operating area (SOA) of the SiC MOSFET-CMF20120D from CREE by considering the maximum allowed drain current according with switching frequency and heatsink thermal impedance variation for 2L-VSI applications which are using sinusoidal PWM

Selecting the operating point A from the SOA (Fig. 8), for a heatsink thermal impedance Z_{th1}=3K/W and a switching frequency of 50 kHz, the maximum allowed drain current is 22 A. If the application requires a higher current for the same switching frequency (e.g. 30 A for 50 kHz, point B) or a higher switching frequency for the same current (e.g. 87 kHz for 22 A, point C) the thermal impedance of the heatsink has to be decreased to Z_{th2}=2 K/W, otherwise the physical thermal limitations of the device are exceeded. Moreover, Fig. 9 emphasizes this problem in more details, if the operating point A is exceeded from switching frequency point of view, by keeping the same heatsink thermal impedance of Z_{th1}=3K/W and the same current I_D=22 A. Fig. 9 shows that for a switching frequency up to 50kHz, the device is not exceeding the maximum allowed limits of case and junction temperature. If the f_{sw} is increased to 70 kHz, the thermal limitations of the device are exceeded, this involving device failure. From losses sharing point of view, as it was expected, by increasing the switching frequency and keeping the same load current, only switching losses are increasing as the conduction losses remain the same.

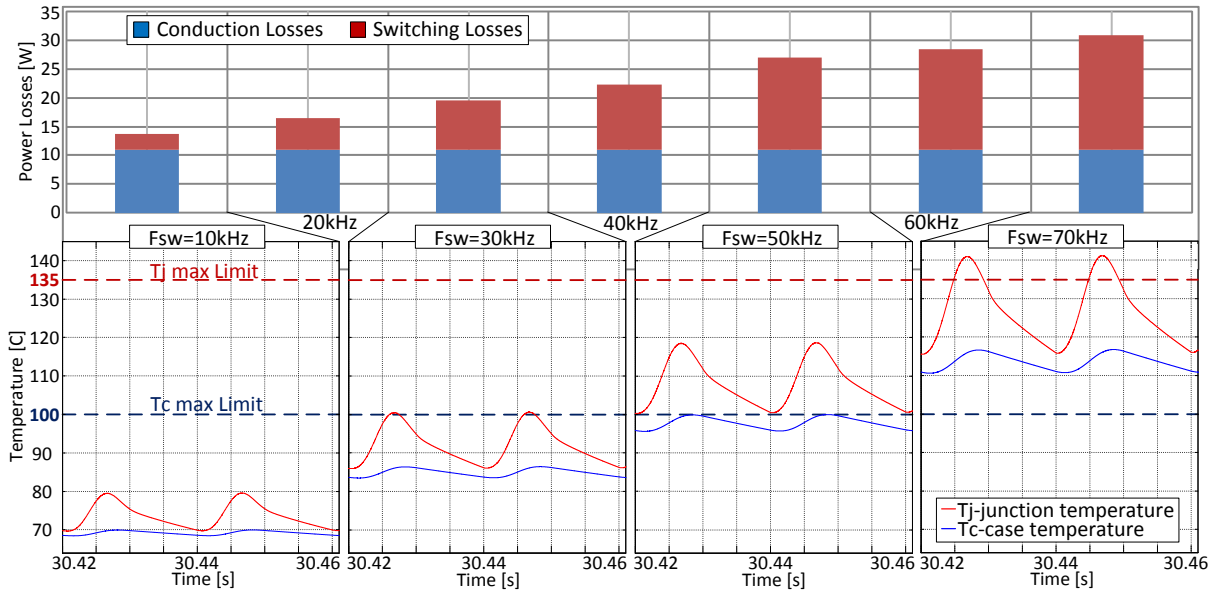


Fig. 9: Conduction and switching losses sharing by increasing the switching frequency for the same drain current of 22A and the corresponding thermal cycling variation of the MOSFET junction and case temperatures for a thermal impedance Z_{th} heatsink of 3 K/W and ambient temperature of 30°C

Finally, a transient study of the MOSFET thermal loading is also performed by considering the conditions of the operating point A. Two main aspects are considered when dealing with dynamics response of the device junction and case temperature, first the ambient temperature is changed from 25°C to 30°C at time 30.56 s and second the load current is changed from 22A to 17A at time 31s. According to the obtained results shown in Fig. 10, it is worth to mention that, after 0.3s (0.58s) from

the mentioned T_a step (I_D load current step), the junction temperature T_j is stabilizing at 118.4°C (92.7°C) and the case temperature at T_c=100°C (82°C).

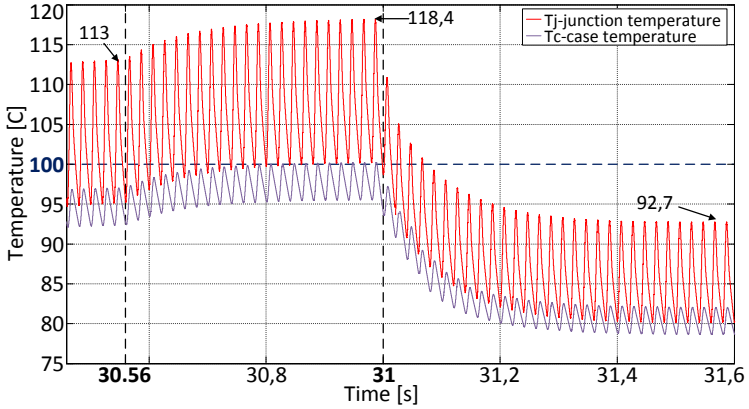


Fig. 10: Transient response of the thermal cycling variation of the junction and case temperatures when the ambient temperature T_a is changing from 25°C to 30°C at time 30.56 s and the device current I_D is changing from 22A to 17A at time 31s

Conclusion

A novel Electro-Thermal Model for the new generation of power electronics WBG devices has been implemented by considering the SiC MOSFET-CMF20120D from CREE. The proposed Device-Model estimates the voltage drop across the device and the switching energies as a function of device current, the off-state blocking voltage and junction temperature variation. The validation of the device model has been performed by comparing the estimated parameters with the ones provided by the datasheet. Moreover, the proposed Thermal-Model is able to consider the thermal coupling within the MOSFET and its freewheeling diode integrated on the same package, and the influence of the ambient temperature variation. The proposed model validation has been achieved by obtaining similar results with a model built in Matlab/Simulink and Plecs toolbox, when the same conditions were applied. The obtained results emphasized the importance of using the temperature loop feedback in order to improve the accuracy of the device junction and case temperature estimation. Afterwards, a case study has been implemented in order to highlight the results concerning the thermal coupling between the MOSFET and the diode. Moreover, the SOA of the SiC MOSFET has been determined for 2L-VSI applications which are using sinusoidal PWM. Thus, by considering the heatsink thermal impedance, the switching frequency and the ambient temperature, the maximum allowed drain current has been determined in order not to exceed the thermal limitations of the device. Finally, the dynamic study of MOSFET junction and case temperature has been also performed by considering the variation of the ambient temperature and of the load current.

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